



## Semarak International Journal of Electronic System Engineering

Journal homepage:  
<https://semarakilmu.my/index.php/sijese/index>  
ISSN: 3030-5519



# Different Asymmetric DC Configuration in Reduced-Switch Multilevel Inverter: A Comparative Topological Analysis

Siti Khodijah Mazalan<sup>1,2</sup>, Baharuddin Ismail<sup>1,2\*</sup>, Zainuddin Mat Isa<sup>1,2</sup>, Muzamir Isa<sup>1</sup>, Syahril Noor Shah<sup>1</sup>, Md. Hairul Nizam Talib<sup>3</sup>

<sup>1</sup> Faculty of Electrical Engineering & Technology, Universiti Malaysia Perlis, Pauh Putra Campus, 02600 Arau, Perlis, Malaysia

<sup>2</sup> Centre of Excellence for Renewable Energy, Universiti Malaysia Perlis, Pauh Putra Campus, 02600 Arau, Perlis, Malaysia

<sup>3</sup> Faculty of Electrical Engineering, Universiti Teknikal Malaysia Melaka, Hang Tuah Jaya, 76100 Durian Tunggal, Melaka, Malaysia

### ARTICLE INFO

#### Article history:

Received 15 December 2024

Received in revised form 27 December 2024

Accepted 22 January 2025

Available online 15 March 2025

#### Keywords:

Multilevel inverter; reduced-switch; THD; asymmetric DC source

### ABSTRACT

Multilevel inverters are becoming more appealing by eliminating the need for filter circuits. As a result, this type of inverter can reduce total harmonic and improve output waveform quality. However, it causes a large number of switches, so a reduced-switch topology is used for a compact and cost-effective inverter. This paper examines a different DC source and switching circuit arrangement for 15-level reduced-switch multilevel inverters (RSMLI). PSIM software is used to model both circuits. The goal is to observe and comprehend the differences in the number of DC sources, switches, and circuit complexity for the same level inverter and to understand how these parameters affect inverter performance. According to the findings, the formulation of the number of DC voltage counts, its switching circuit, and structure arrangement all have a different effect on RSMLI reliability.

## 1. Introduction

Since many industrial applications require power converters, electrical power conversion is important in electrical systems. Multilevel inverters (MLI) are well known for their ability to increase voltage level, with higher level MLI providing better sinusoid output resolution [16,7,8]. MLI provided solutions for many applications such as traction systems, industrial machinery, and renewable energy systems [22,10,24]. MLI, as opposed to conventional 2-level inverters, can operate at fundamental switching frequency, resulting in lower switching and conduction losses per operation [20,19,25]. MLIs have three traditional topologies: cascaded H-bridge, diode clamped, and flying capacitor [5,14,17]. From those three, cascaded H-bridge is preferred for a higher voltage application [21,1,6].

The main elements that comprise a multilevel inverter (MLI) topology are power switches. In addition to these switches, passive components such as inductors, capacitors, and transformers are used to explore a range of MLI topologies. However, the disadvantages of passive components,

\*Baharuddin Ismail

E-mail address: [baha@unimap.edu.my](mailto:baha@unimap.edu.my)

particularly transformers and capacitors, are that they are typically heavy and large in size [11,23], resulting in a bulky inverter and adding extra cost to the overall inverter [15]. These concerns incited the idea of reducing the size of the inverter. The structure is remodeled by utilizing a reduced number of switches and the redundant switching sequence. With this focus, modified multilevel topology first appeared and later known as reduced-switch MLI (RSMLI). The RSMLI was further investigated in symmetrical and asymmetrical modelling [14,18]. Asymmetrical MLI structures have unequal DC source values, while symmetrical MLI structures have equal DC source values [19]. Despite the fact that the reduced-switch topology varies the number of DC sources and switches, this structural modification allows for a higher-level output in a compact size [3,2,9]. The design goal is to produce a higher number of levels with fewer switches while maintaining reasonable voltage stress on the switches for inverter reliability.

Since the passive component is not considered in this paper, the structural focus is on H-bridge inspired MLI. In a typical cascaded H-bridge inverter topology, the level-up is achieved by cascading the  $n$ th H-bridge module [6], which it is made up of four switches. According to the power conversion principle, the four switches form two complementary pairs of switches to conduct current to the output while avoiding short circuits. The polarity of MLI is changed by turning one of its complementary pair switches on and off alternately. Both RSMLI topologies in this paper use a modified H-bridge configuration.

The aim of this paper is to analyses RSMLI topologies with the same output levels but a different number of switches, DC source count, and ratio. Both are 15-level asymmetrical RSMLI topologies adapted from [4] and [13].

- i) The study demonstrated 15-level reduced-switch multilevel inverter topologies in asymmetrical DC source configuration.
- ii) The switching signal is presented for each 15-level reduced-switch multilevel inverter.
- iii) Important parameters such as voltage stress, modulation index and output voltage are expressed mathematically.
- iv) The circuit complexity is compared in terms of the combination of unidirectional and bidirectional switches.
- v) The RSMLI's circuit reliability is compared in terms of the highest rating switches and total voltage stress for the topology.

The rest of the paper is organized as follows. In Section 2, working principle with related mathematical expression for the comparative topologies are described. Then, the components in both topologies are tabulated for evaluation. Some simulation results are given in Section 3. Finally, conclusions are drawn on Section 4.

## **2. Comparative Topology**

A RSMLI topology in a circuit typically consists of multiple DC voltage sources and switching device arrays. A combination of unidirectional and bidirectional switches is typically synthesized to isolate multiple DC sources in a single circuit. A unidirectional switch consists of a power switch and an anti-parallel diode capable of blocking voltage while conducting current in both polarities. Meanwhile, a bidirectional switch made up of two power switches typically adds to the RSMLI circuit complexity. This type of switch can conduct current in both directions while also blocking positive or negative voltage during the Off-state.

Topology I composed of ten-switches single-phase RSMLI circuit with six unidirectional switches  $S_1, S_2, S_3, S_5, S_6, S_7$  and two bidirectional switches  $S_4, S_8$ . The levels are generated by directing the DC sources of  $V_{DC1}, V_{DC2}, V_{DC3}$ , and  $V_{DC4}$  through a different set of switching commutation. Figure 1 shows the schematic of Topology I.

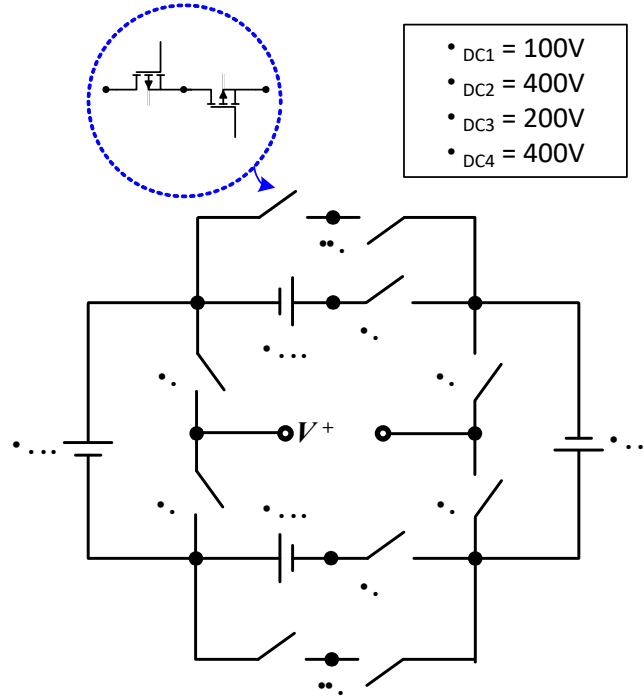


Fig. 1. Schematic of Topology I as adapted from [4]

## 2.1 The Algorithm of Topology I

The DC voltage values as follow Eq. (1),

$$V_{DC1} = 100V, V_{DC2} = 400V, V_{DC3} = 200V, V_{DC4} = 400V \quad (1)$$

The asymmetric DC voltage is composed to yield each staircase level for a positive level output as in Table 1. The voltage value is made in per unit for a simplification,

**Table 1**

Mathematical expression of per level voltage

Staircase level	Per level voltage (positive voltage level)
Level I	$V_1 = V_{DC1} = 1V_{pu}$
Level II	$V_2 = V_{DC3} = 2V_{pu}$
Level III	$V_3 = V_{DC1} + V_{DC3} = 3V_{pu}$
Level IV	$V_4 = V_{DC4} = 4V_{pu}$
Level V	$V_5 = V_{DC1} + V_{DC4} = 5V_{pu}$
Level VI	$V_6 = V_{DC3} + V_{DC4} = 6V_{pu}$
Level VII	$V_7 = V_{DC1} + V_{DC3} + V_{DC4} = 7V_{pu}$

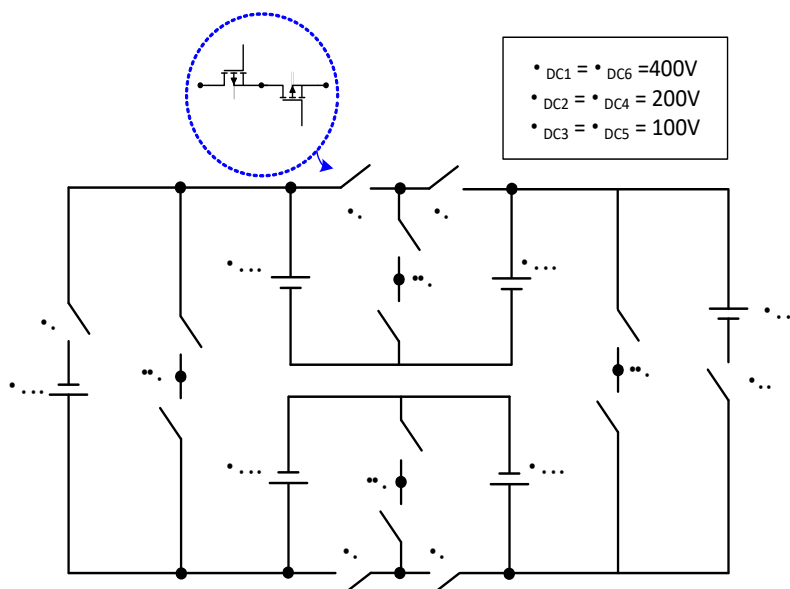
Different combinations of DC voltages are synthesized to composed for negative output levels.  $V_{DC1} = 100V, V_{DC3} = 200V, V_{DC4} = 400V$  are for positive level while  $V_{DC1} = 100V, V_{DC2} = 400V, V_{DC3} = 200V$

are composed for the negative side. All the positive and negative level were obtained and summarized in Table 2.

**Table 2**  
Switching state for 15-level single-phase RSMLI (Topology I)

Polarity complementary switches				Level complementary & voltage level switches				MLI output
$S_1$	$S_2$	$S_5$	$S_6$	$S_3$	' $S_4$	$S_7$	' $S_8$	Staircase voltage, $V_o$
1	0	1	0	0	1	0	0	0
1	0	0	1	0	0	0	1	$V_1$
0	1	1	0	0	0	0	1	$V_2$
1	0	1	0	0	0	0	1	$V_3$
0	1	0	1	0	0	1	0	$V_4$
1	0	0	1	0	0	1	0	$V_5$
0	1	1	0	0	0	1	0	$V_6$
1	0	1	0	0	0	1	0	$V_7$
1	0	1	0	0	1	0	1	0
0	1	1	0	0	1	0	0	$-V_1$
1	0	0	1	0	1	0	0	$-V_2$
0	1	0	1	0	1	0	0	$-V_3$
1	0	1	0	1	0	0	0	$-V_4$
0	1	1	0	1	0	0	0	$-V_5$
1	0	0	1	1	0	0	0	$-V_6$
0	1	0	1	1	0	0	0	$-V_7$

The single-phase RSMLI structure of Topology II as shown in Figure 2 comprises of fourteen switches and six DC voltage sources as in Figure 2. The polarity and level generation in made by a combination of six unidirectional switches  $S_1, S_3, S_6, S_8, S_9, S_{10}$ , four bidirectional switches ' $S_2, S_4, S_5, S_7$ '. By controlling the DC sources of  $V_{DC1}, V_{DC2}, V_{DC3}, V_{DC4}, V_{DC5}$  and  $V_{DC6}$  via a different set of current paths yields a 15-level RSMLI output.



**Fig. 2.** Schematic of Topology II as adapted from [13]

## 2.2 The Algorithm of Topology II,

The DC voltage values for Topology II is given by Eq. (2),

$$V_{DC1} = 400V, V_{DC2} = 200V, V_{DC3} = 100V, V_{DC4} = 200V, V_{DC5} = 100V, V_{DC6} = 400V \quad (2)$$

The asymmetric DC voltage is composed to yield each staircase level for a positive level output as in Table 3. The voltage value is made in per unit for a simplification,

**Table 3**

Mathematical expression of per level voltage

Staircase level	Per level voltage (positive voltage level)
Level I	$V_1 = V_{DC5} = 1V_{pu}$ ,
Level II	$V_2 = V_{DC4} = 2V_{pu}$ ,
Level III	$V_3 = V_{DC4} + V_{DC5} = 3V_{pu}$ ,
Level IV	$V_4 = V_{DC6} = 4V_{pu}$ ,
Level V	$V_5 = V_{DC5} + V_{DC6} = 5V_{pu}$ ,
Level VI	$V_6 = V_{DC4} + V_{DC6} = 6V_{pu}$ ,
Level VII	$V_7 = V_{DC4} + V_{DC5} + V_{DC6} = 7V_{pu}$

Then, different combinations of DC voltages are synthesized to composed for negative output levels.  $V_{DC1} = 400V$ ,  $V_{DC2} = 200V$ ,  $V_{DC3} = 100V$  are for positive level while  $V_{DC4} = 400V$ ,  $V_{DC5} = 200V$ ,  $V_{DC6} = 100V$  are composed for the negative side. All the positive and negative polarities are achieved with alternate combination of switches and summarized in Table 4.

**Table 4**

Switching state for 15-level single-phase RSMLI (Topology II)

Polarity Complementary switches				Level Complementary & voltage level switches						MLI Output
$S_1$	$S_3$	$S_6$	$S_8$	$S_2$	$S_4$	$S_5$	$S_7$	$S_9$	$S_{10}$	Staircase voltage, $V_o$
1	0	1	0	0	0	1	0	0	0	0
1	0	0	1	1	0	0	1	0	1	$V_1$
0	1	1	0	0	0	0	0	0	1	$V_2$
1	0	1	0	0	0	0	0	0	1	$V_3$
0	1	0	1	1	0	0	1	1	0	$V_4$
1	0	0	1	1	0	0	1	1	0	$V_5$
0	1	1	0	0	0	0	0	1	0	$V_6$
1	0	1	0	0	0	0	0	1	0	$V_7$
1	0	1	0	0	0	1	0	0	1	0
0	1	1	0	0	0	1	0	0	0	$-V_1$
1	0	0	1	1	0	1	1	0	0	$-V_2$
0	1	0	1	1	0	1	1	0	0	$-V_3$
1	0	1	0	0	1	0	0	0	0	$-V_4$
0	1	1	0	0	1	0	0	0	0	$-V_5$
1	0	0	1	1	1	0	1	0	0	$-V_6$
0	1	0	1	1	1	0	1	0	0	$-V_7$

## 2.3 RSMLI's Voltage Stress

By arranging a combination of DC Source and switches, several RSMLI topologies can be obtained. The value of voltage stress across the switches is an important variable in evaluating RSMLI reliability

[12]. To simplify the calculation, voltage expression in Eqs. (1)-(2) are considered in  $V_{pu}$ . The voltage stress calculation for each corresponding circuit is computed as in Eqs. (3)-(10). *Total Blocking Voltage (TBV)<sub>pu</sub>* for Topology I is given by,

Topology 1,

a. Unidirectional switches,

$$\left. \begin{aligned} S_1 = S_2 = V_{DC1} &= V_{pu} \\ S_5 = S_6 = V_{DC3} &= 2 V_{pu} \\ S_3 = S_4 = V_{DC1} + V_{DC2} + V_{DC3} + V_{DC4} &= 11 V_{pu} \end{aligned} \right\} \quad (3)$$

b. Bidirectional switches,

$$S_4 = S_8 = V_{DC1} + V_{DC2} + V_{DC3} = 7 V_{pu} \quad (4)$$

Then,

$$\therefore TBV_{pu} = (2 * V_{pu}) + (2 * 2V_{pu}) + (2 * 11V_{pu}) + (4 * 7V_{pu}) = 56 V_{pu} \quad (5)$$

Thus, the maximum blocking voltage (MBV) is given,

$$\therefore \text{Highest switch rating, } MBV = 11 V_{pu} \quad (6)$$

Topology 2,

*TBV* for Topology II is given by,

a. Unidirectional switches,

$$\left. \begin{aligned} S_1 = S_3 = 2V_{DC2} &= 4 V_{pu} \\ S_6 = S_8 = 2V_{DC1} &= 2 V_{pu} \\ S_9 = S_{10} = 2(V_{DC1} + V_{DC2} + V_{DC3}) &= 12 V_{pu} \end{aligned} \right\} \quad (7)$$

b. Bidirectional switches,

$$\left. \begin{aligned} S_2 = V_{DC2} &= 2 V_{pu} \\ S_4 = S_5 = 2(V_{DC1} + V_{DC2}) + V_{DC3} &= 9 V_{pu} \\ S_7 = V_{DC1} &= V_{pu} \end{aligned} \right\} \quad (8)$$

$$\therefore TBV_{pu} = (2 * 4V_{DC}) + (2 * 2V_{DC}) + (2 * 12V_{DC}) + (2V_{DC}) + (2 * 9V_{DC}) + (V_{DC}) = 57 V_{pu} \quad (9)$$

Thus, the maximum blocking voltage (MBV) is given by,

$$\therefore \text{Highest switch rating, } MBV = 12 V_{pu} \quad (10)$$

## 2.4 The comparison analysis

Table 5 shows the comparison of both RSMLI topologies presented in this paper. All the comparison is made in extended three-phase concept. The three-phase simulation results for Topology I and II are shown Section 3.

**Table 5**  
Comparison of Three-phase RSMLI topologies

	Topology I	Topology II
Three-phase voltage level	29	29
Number of switches	30	42
Number of DC source	12	18
DC source ratio progression	Binary 1:2:4	Binary 1:2:4
Maximum number of On-state switches	9	9
Highest rating switches	11 $V_{pu}$	12 $V_{pu}$
Total blocking voltage	168	171
Circuit complexity	18 unidirectional	18 unidirectional
(unidirectional/bidirectional switches)	6 bidirectional	12 bidirectional
Symmetry/ Asymmetry	Asymmetry	Asymmetry

## 2.5 Modulation strategy

Simulation model for both topologies is performed on PSIM in an extended model of three-phase and fundamental frequency modulation. The amplitude of the  $n$ th harmonic of the inverter phase voltage can be obtained from the sum of the output voltages in Eq. (11),

$$\begin{aligned}
 V_{AN} &= \frac{4V_{DC}}{n\pi} ((V_{DC1}\cos(\alpha_1) + V_{DC2}\cos(\alpha_2) + V_{DC3}\cos(\alpha_3) + V_{DC4}\cos(\alpha_4) + \\
 &V_{DC5}\cos(\alpha_5) + V_{DC6}\cos(\alpha_6) + V_{DC7}\cos(\alpha_7)) \\
 V_{AN} &= \frac{4V_{DC}}{n\pi} ((V_{DC1}\cos(5\alpha_1) + V_{DC2}\cos(5\alpha_2) + V_{DC3}\cos(5\alpha_3) + V_{DC4}\cos(5\alpha_4) + \\
 &V_{DC5}\cos(5\alpha_5) + V_{DC6}\cos(5\alpha_6) + V_{DC7}\cos(5\alpha_7)) \\
 &\vdots \\
 V_{AN} &= \frac{4V_{DC}}{n\pi} ((V_{DC1}\cos(19\alpha_1) + V_{DC2}\cos(19\alpha_2) + V_{DC3}\cos(19\alpha_3) + \\
 &V_{DC4}\cos(19\alpha_4) + V_{DC5}\cos(19\alpha_5) + V_{DC6}\cos(19\alpha_6) + V_{DC7}\cos(19\alpha_7))
 \end{aligned} \quad (11)$$

where,  $\alpha_1, \alpha_2, \dots$  are switching angles  
and  $V_{AN}(t) = V_1(t) + V_5(t) + \dots + V_{19}(t)$

Hence, Total Harmonic Distortion (THD) is given by Eq. (12),

$$THD = \frac{\sqrt{\sum_{n=5,7,11\dots}^{49} (V_n)^2}}{V_1} \quad (12)$$

where,  $V_1$  is a fundamental voltage and  $V_n$  are voltages of the  $n$ th harmonic

The obtained switching angles by varying  $0.4 < M_i < 0.8$  are as in Table 6. These values are calculated based on the non-linear component in Eq. (11) and the system's THD are calculated by using Eq. (12).

**Table 6**

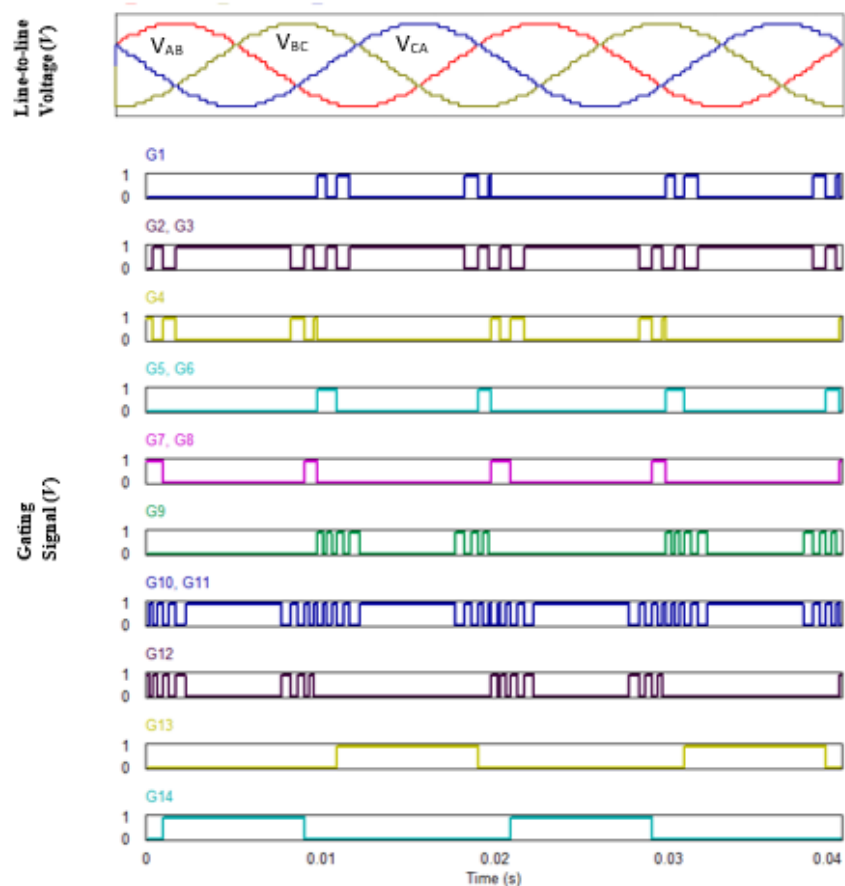
Switching angles result with varying modulation indices

$M_i$	$\alpha_1$	$\alpha_2$	$\alpha_3$	$\alpha_4$	$\alpha_5$	$\alpha_6$	$\alpha_7$	THD
0.40	34.62	43.74	52.99	63.51	75.29	89.00	89.00	5.92
0.45	34.89	41.36	50.54	58.91	68.66	80.40	89.00	4.58
0.50	33.77	41.16	48.94	56.94	65.67	75.46	87.12	4.96
0.55	21.37	35.24	48.42	53.76	62.93	70.45	89.00	4.21
0.60	14.13	25.86	38.61	52.61	58.66	67.24	89.00	3.77
0.65	11.34	28.41	38.80	45.59	58.70	61.40	77.68	3.74
0.70	6.20	21.43	31.99	42.80	49.60	61.45	74.51	2.89
0.75	1.00	9.00	14.11	22.93	32.16	43.27	89.00	2.73
0.80	7.63	13.01	21.07	27.90	39.46	55.13	62.45	2.59

### 3. Results

#### 3.1 Voltage Profile

This section discusses the results obtained from the simulation study. A SHEPWM modulation is used with selected modulation index solution of 0.8 from Table 4. The gating signal of Topology I and II are shown in Figure 3 and Figure 4 to demonstrate the three-phase RSMLI for Topology I and II structures.



**Fig. 3.** Gating signal for Topology I

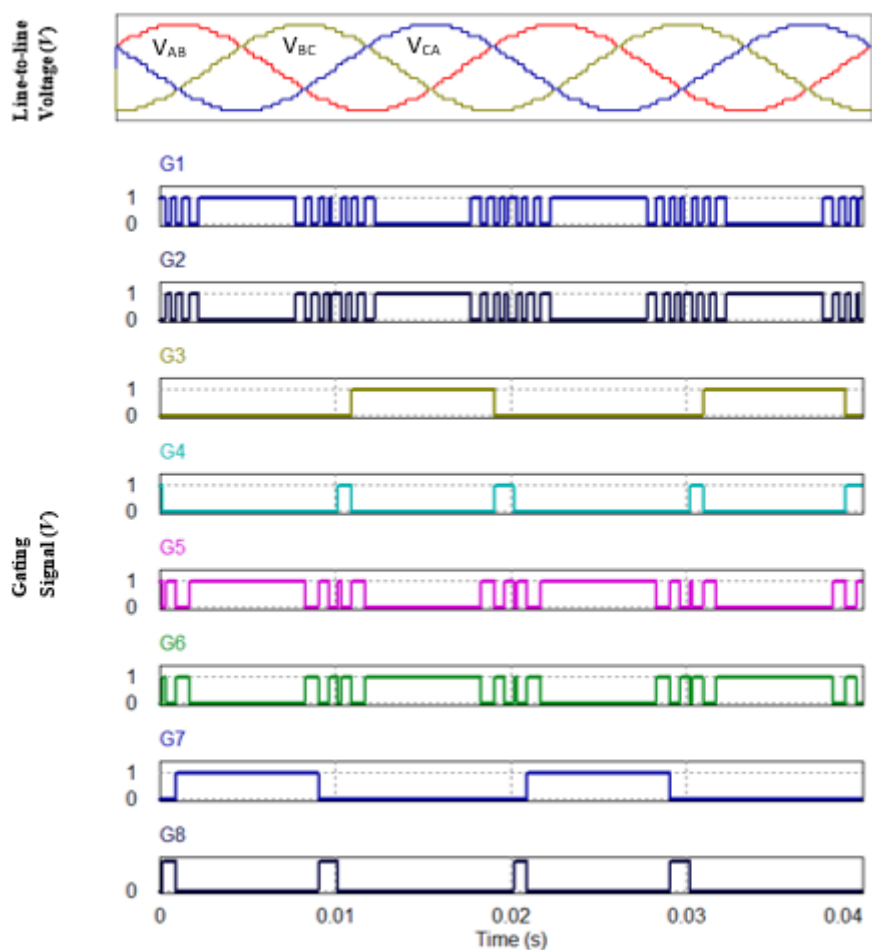


Fig. 4. Gating signal for Topology II

Both topologies run in fundamental frequency modulation with  $M_i$  of 0.8 and Figure 5 shows a compatible three phase output voltage which is similar for Topology I and II.

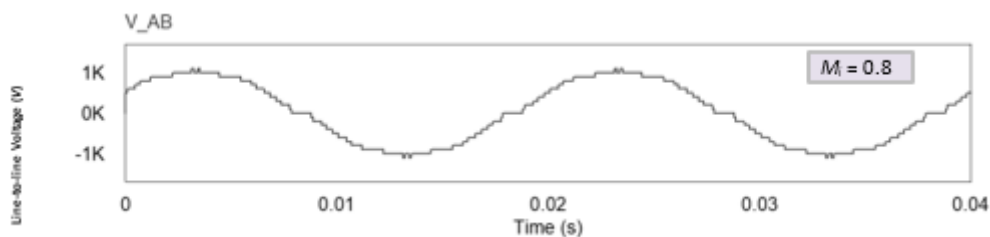
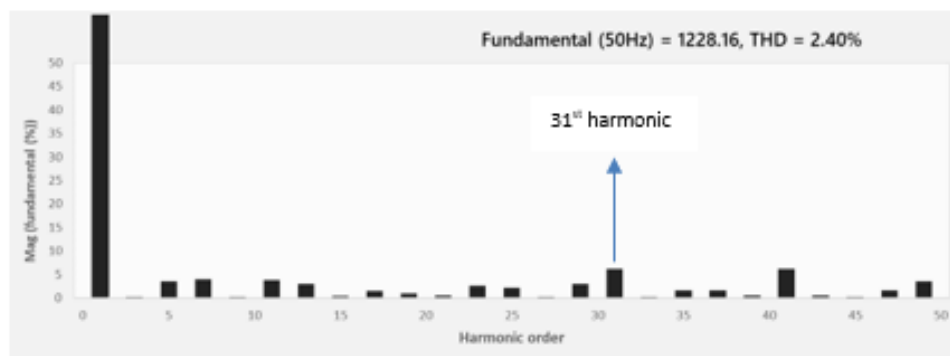


Fig. 5. Line-to-line output voltage of three-phase multilevel inverter

### 3.2 Harmonic Profile

Figure 6 shows the obtained harmonic profile. The first significant harmonic that exceed 8% is at the 31<sup>st</sup> harmonics. The total harmonic distortion (THD) is 2.4% for both topologies.



**Fig. 6.** FFT analysis for Selective Harmonic Elimination at modulation index value of 0.8

#### 4. Conclusions

This paper compares two reduced-switch multilevel inverter topologies with an asymmetrical structure. The magnitude voltage and harmonic profile for both structures are analysed. Based on the comparisons, Topology I provide a better structure than Topology II; moreover, the fact that Topology II has two additional DC sources does not reduce circuit stress. Each topology has the same number of on-state switches and reasonable voltage stress. Topology I have the fewest number of circuit components and the lowest maximum switch rating of  $11 V_{pu}$ . Despite having a different number of DC sources and switches, Both RSMLI circuits produce the same output voltage with a reduced THD of 2.4%.

From the analysis, has helps to compute six design consideration to model a new reduced-switch topology. As such, the design considerations are:

- i) The number of voltage level for a new reduced-switch multilevel inverter topology
- ii) Symmetric or asymmetric DC source configurations and ratio progression
- iii) Switches combination to compute voltage level
- iv) Switches combination to control circuit polarity
- v) Unidirectional or bidirectional type of switches to control current direction
- vi) Isolation of the multiple DC sources in single circuit to prevent circuit error, short circuit and reverse voltages.
- vii) The rating of switches, switching sequence, on-state switches, and switching distribution to yield the desired voltage level of reduced-switch multilevel inverter.

As to conclude, the design criteria of Topology I and Topology II as well as its output and harmonic profile are summarized in this paper.

#### 5. Acknowledgement

The authors would like to acknowledge the support from the Fundamental Research Grant Scheme (FRGS) under a grant number of the Fundamental Research Grant Scheme FRGS/1/2020/TKO/UNIMAP/03/17 from the Ministry of Education Malaysia.

## References

- [1] Ahmad, Salman, Atif Iqbal, Imtiaz Ashraf, and Mohammad Meraj. 2022. "Improved Power Quality Operation of Symmetrical and Asymmetrical Multilevel Inverter Using Invasive Weed Optimization Technique." *Energy Reports* 8: 3323–36. <https://doi.org/10.1016/j.egy.2022.01.122>
- [2] Anand, Vishal, and Varsha Singh. 2020. "Compact Symmetrical and Asymmetrical Multilevel Inverter with Reduced Switches." *Int Trans Electr Energ Syst* 30 (April): 1–20. <https://doi.org/10.1002/2050-7038.12458>
- [3] Arif, M. Saad Bin, Uvais Mustafa, Shahrin Bin Md Ayob, Jose Rodriguez, Abdul Nadeem, and Mohamed Abdelrahman. 2021. "Asymmetrical 17-Level Inverter Topology with Reduced Total Standing Voltage and Device Count." *IEEE Access* 9: 69710–23. <https://doi.org/10.1109/ACCESS.2021.3077968>
- [4] Babaei, Ebrahim, and Sara Laali. 2016. "New Extendable 15-Level Basic Unit for Multilevel Inverters." *Journal of Circuits, Systems and Computers* 25 (12). <https://doi.org/10.1142/S0218126616501516>
- [5] Barah, Sushree Smrutimayee, and Sasmita Behera. 2021. "An Optimize Configuration of H-Bridge Multilevel Inverter." *ICPEE 2021 - 2021 1st International Conference on Power Electronics and Energy* 1 (1): 7–10. <https://doi.org/10.1109/ICPEE50452.2021.9358533>
- [6] Hamad, Hassan Salman. 2020. "Implementation of the Conventional Seven-Level Single-Phase Symmetrical Cascaded H-Bridge MLI Based on PSIM." *International Journal of Power Electronics and Drive Systems* 11 (1): 169–77. <https://doi.org/10.11591/ijpeds.v11.i1.pp169-177>
- [7] Hiendro, Ayong, Ismail Yusuf, Junaidi, F. Trias Pontia Wigiyanto, and Yohannes M. Simanjuntak. 2020. "Optimization of SHEPWM Cascaded Multilevel Inverter Switching Patterns." *International Journal of Power Electronics and Drive Systems* 11 (3): 1570–78. <https://doi.org/10.11591/ijpeds.v11.i3.pp1570-1578>
- [8] Hosseinpour, Majid, S. Mansoori, and H. Shayeghi. 2020. "Selective Harmonics Elimination Technique in Cascaded H-Bridge Multi-Level Inverters Using the Salp Swarm Optimization Algorithm." *Journal of Operation and Automation in Power Engineering* 8 (1): 32–42.
- [9] Khodijah, S., Baharuddin Ismail, Muzamir Isa, M. Syahril, and M. N.K.H. Rohani. 2020. "Performance Analysis of a Modified Reduce Component Count Multilevel Inverter." *Journal of Physics: Conference Series* 1432 (1). <https://doi.org/10.1088/1742-6596/1432/1/012018>
- [10] Kubendran, V, Y Mohamed Shuaib, and J Preetha Roselyn. 2022. "Development of Multilevel Inverter with Reduced Switch Counts and Limited Sources for Electric Vehicles." *Sustainable Energy Technologies and Assessments* 52 (PD): 102332. <https://doi.org/10.1016/j.seta.2022.102332>
- [11] Leon, Jose I., Samir Kouro, Leopoldo G. Franquelo, Jose Rodriguez, and Bin Wu. 2016. "The Essential Role and the Continuous Evolution of Modulation Techniques for Voltage-Source Inverters in the Past, Present, and Future Power Electronics." *IEEE Transactions on Industrial Electronics* 63 (5): 2688–2701. <https://doi.org/10.1109/TIE.2016.2519321>
- [12] Masaoud, Ammar, Hew Wooi Ping, Saad Mekhilef, and Senior Member. 2014. "New Three-Phase Multilevel Inverter With Reduced Number of Power Electronic Components." *IEEE Transactions on Power Electronics* 29 (11): 6018–29. <https://doi.org/10.1109/TPEL.2014.2298616>
- [13] Masoudina, F, E Babaei, M Sabahi, and H Alipour. 2020. "New Cascaded Multilevel Inverter with Reduced Power Electronic Components." *Iranian Journal of Electrical and Electronic Engineering* 16 (1): 107–13. <https://doi.org/10.1080/00207217.2020.1726484>
- [14] Nanda, Lipika, Chitralekha Jena, Arjyadhara Pradhan, and Babita Panda. 2022. "A Proposed Asymmetrical Configuration of Cascaded Multilevel Inverter Topology for High Level Generation." *International Journal of Power Electronics and Drive Systems* 13 (1): 289–97. <https://doi.org/10.11591/ijpeds.v13.i1.pp289-297>
- [15] Prabakaran, Natarajan, and Kaliannan Palanisamy. 2017. "Analysis of Cascaded H-Bridge Multilevel Inverter Configuration with Double Level Circuit" 10: 1023–33. <https://doi.org/10.1049/iet-pel.2016.0506>
- [16] Prayagl, Aparna. 2016. "A Comparative Analysis of Classical Three Phase Multilevel (Five Level) Inverter Topologies," 1–5. <https://doi.org/10.1109/ICPEICES.2016.7853567>
- [17] Rodríguez, José, Senior Member, Jih-sheng Lai, and Senior Member. 2002. "Multilevel Inverters : A Survey of Topologies , Controls , and Applications" 49 (4): 724–38. <https://doi.org/10.1109/TIE.2002.801052>
- [18] Sabyasachi, Sidharth, Student Member, and Vijay B Borghate. 2017. "Hybrid Control Technique-Based Three-Phase Cascaded Multilevel Inverter Topology" 5. <https://doi.org/10.1109/ACCESS.2017.2727551>
- [19] Saleh, Wail Ali Ali, Nurul Ain Mohd Said, and Wahidah Abd Halim. 2020. "Harmonic Minimization of a Single-Phase Asymmetrical TCHB Multilevel Inverter Based on Nearest Level Control Method." *International Journal of Power Electronics and Drive Systems* 11 (3): 1406–14. <https://doi.org/10.11591/ijpeds.v11.i3.pp1406-1414>
- [20] Seifi, Ali, Majid Hosseinpour, Abdolmajid Dejamkhooy, and Farzad Sedaghati. 2020. "Novel Reduced Switch-Count Structure for Symmetric/Asymmetric Cascaded Multilevel Inverter." *Arabian Journal for Science and Engineering* 45 (8): 6687–6700. <https://doi.org/10.1007/s13369-020-04659-4>

- [21] Thakre, Kishor, Kanungo Barada, and Vinaya Sagar. 2022. "Modified Cascaded Multilevel Inverter for Renewable Energy Systems with Less Number of Unidirectional Switches." *Energy Reports* 8: 5296–5304. <https://doi.org/10.1016/j.egy.2022.03.167>
- [22] Trabelsi, Mohamed, Hani Vahedi, and Haitham Abu-Rub. 2021. "Review on Single-DC-Source Multilevel Inverters: Topologies, Challenges, Industrial Applications, and Recommendations." *IEEE Open Journal of the Industrial Electronics Society* 2 (January): 112–27. <https://doi.org/10.1109/OJIES.2021.3054666>
- [23] Vemuganti, Hari Priya, Dharmavarapu Sreenivasarao, Siva Kumar Ganjikunta, Hiralal Murlidhar Suryawanshi, and Haitham Abu-Rub. 2021. "A Survey on Reduced Switch Count Multilevel Inverters." *IEEE Open Journal of the Industrial Electronics Society* 2 (January): 80–111. <https://doi.org/10.1109/OJIES.2021.3050214>
- [24] Vijayabaskar, S, D Subramani, K Manoj, and P Vishnuprasanth. 2022. "H-BRIDGE THIRTEEN LEVEL INVERTER USING REDUCED NUMBER OF SWITCHES FOR INDUSTRIAL APPLICATIONS" 7838 (June): 107–12. <https://doi.org/10.36713/epra10399>
- [25] Yarlagadda, Anil Kumar, and Vimlesh Verma. 2022. "A Novel Multilevel Inverter Topology with Reduced Number of Component Count and Total Standing Voltage for Renewable Energy Conversion System." *Renewable Energy Focus* 43: 84–92. <https://doi.org/10.1016/j.ref.2022.09.004>