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Design of CMOS-based Instrumentation Amplifier for Energy Harvesting in Biomedical Application

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ABSTRACT

Biomedical signals usually are very weak due to low amplitude. An instrumentation amplifier which practically applied in biomedical applications is designed due to its numerous advantages such as gain can be adjusted easily by a single control without changing the whole structure and its common-mode rejection ratio (CMRR) is high. This project proposed a three op-amp instrumentation amplifier by using three two-stage complementary metal-oxide-semiconductor (CMOS) operational amplifier and designed with 130 nm CMOS technology. The gain of the proposed amplifier for pre-layout simulation is 64.15 dB with input-referred noise of 10.41 μ(V/$\sqrt{}$Hz) and power dissipation of 115.6 μW and a CMRR of 107.25 dB. The gain of the amplifier for post-layout simulation is 63.69 dB with input-referred noise of 10.52 μ(V/$\sqrt{}$Hz), the power dissipation of 115.6μ W, and CMRR of 100.39 dB. Apart from that, the amplifier is designed with a size layout of 5.25 μm x 104 μm. The circuit designed will be useful to embed together in energy harvesting system for wearable biomedical system.

1. Introduction

Nowadays, instrumentation amplifier is widely used in the in medical application. An instrumentation amplifier is normally used for the measurement of low-frequency signals [1]. Amplifier for ECG should have a gain of 1000 which is 60 dB, and the common-mode rejection ratio (CMRR) should be above 100 dB [1,2]. Low-frequency signals including electrocardiogram (ECG), brain signals, nerve synapses pulses, etc. An amplifier that is equipped with the characteristic of high CMRR is suitable for biomedical applications [3-5]. Hence, low-frequency signals can be amplified along with the rejection of noise. Instrumentation amplifiers can be used to suppress unwanted noise which will affect the original signal [5]. An instrumentation amplifier is very crucial in a biomedical instrumentation system due to its high input impedance and high common-mode rejection ratio [6-8]. Thus, unwanted signals can be rejected efficiently. Since the amplifier plays an important role in the whole system, some criteria are needed to have better performance [9,10]. Normally, the signals are having a very low frequency and come along with the noise and thus the signals are disrupted

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[11,12]. Once the frequency is low, the flicker noise of the transistor will be very high since the flicker noise is inversely proportional to the frequency of the input signal. Furthermore, it also should have criteria of high CMRR. This proofs that an instrumental amplifier also made useful to measure the current when applied together within energy harvesting circuit [13-15] especially for wearable biomedical devices.

Figure 1 shows the schematic diagram of the instrumentation amplifier and Figure 2 shows the biomedical electronics detecting system blocks which including an electrode, amplifier, low pass filter, sample and hold circuit as well as analog-to-digital converter (ADC). The biomedical signal is detected, and the useless interferences may also pick up by the electrode together. Biomedical electronics are unable to detect low amplitude signals. Therefore, application with good performance which consists of high gain, low input-referred noise, low power dissipation is required.

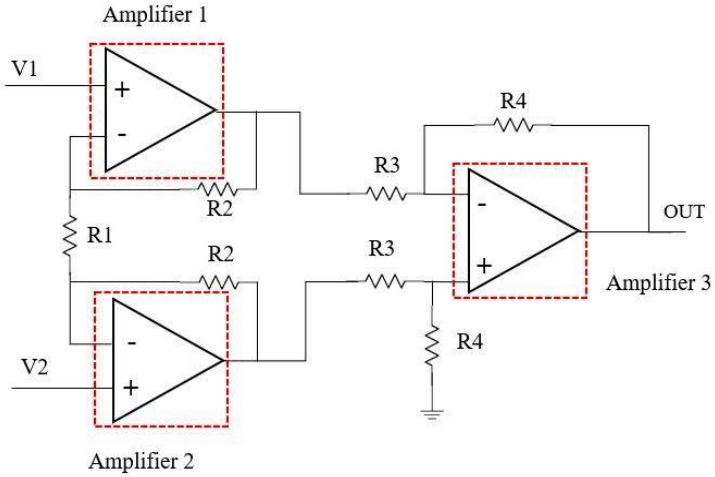


Fig. 1. Schematic diagram of instrumentation amplifier

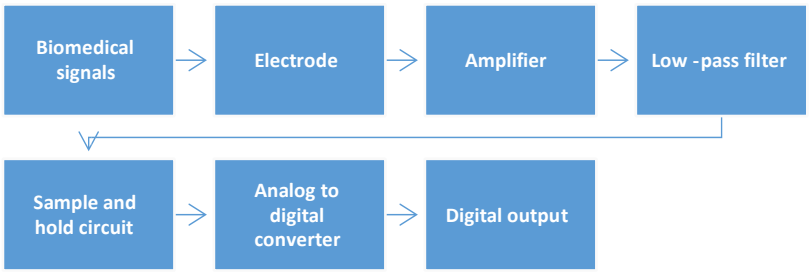


Fig. 2. Biomedical electronics detecting system blocks

2. Amplifier Design

The simulation of CMOS instrumentation amplifier for biomedical application is done using Cadence Software. High noise immunity and low static power consumption can be the most important characteristics of CMOS [10] since the transistor of the Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) pair are off while the other one is on [2]. The amplifier is designed using 130 nm technology with a voltage supply of 1.2 V. Gain and CMRR of the designed amplifier should be above 60 dB and 100 dB respectively [1,2]. Power dissipation and input-referred noise of the designed, m(V/$\sqrt{\ }$Hz) [5] respectively as a reference value for the project to make an improvement.

Figure 3 shows the schematic of the two-stage CMOS op-amp with transistors labelled as M1 to M8, while capacitors, C1 and C2. Then, the design of the overall circuit is encapsulated into an op-

amp circuit as shown in Figure 4. The schematic diagram of the proposed amplifier with the instrumentation amplifier connection as per Figure 1. The circuit is studied, simulated and the performance of the designed circuit which are differential gain, power dissipation, input-referred noise, and CMRR were investigated.

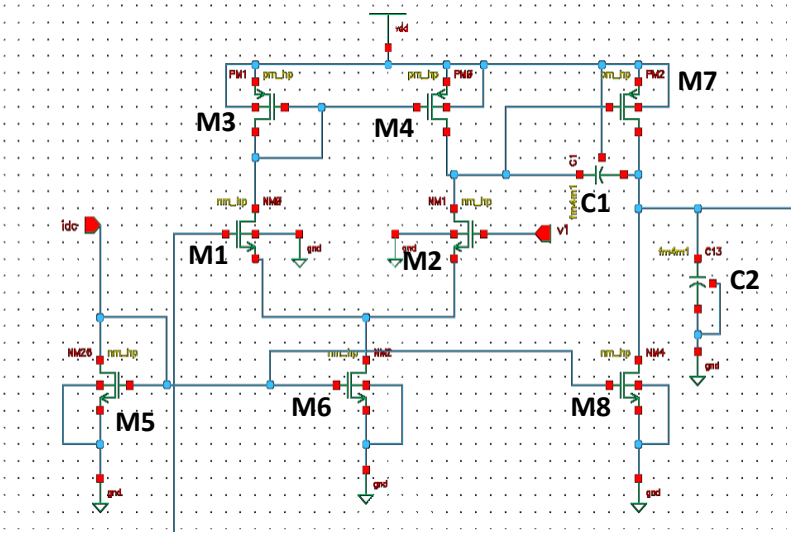


Fig. 3. Schematic of two-stage CMOS op-amp

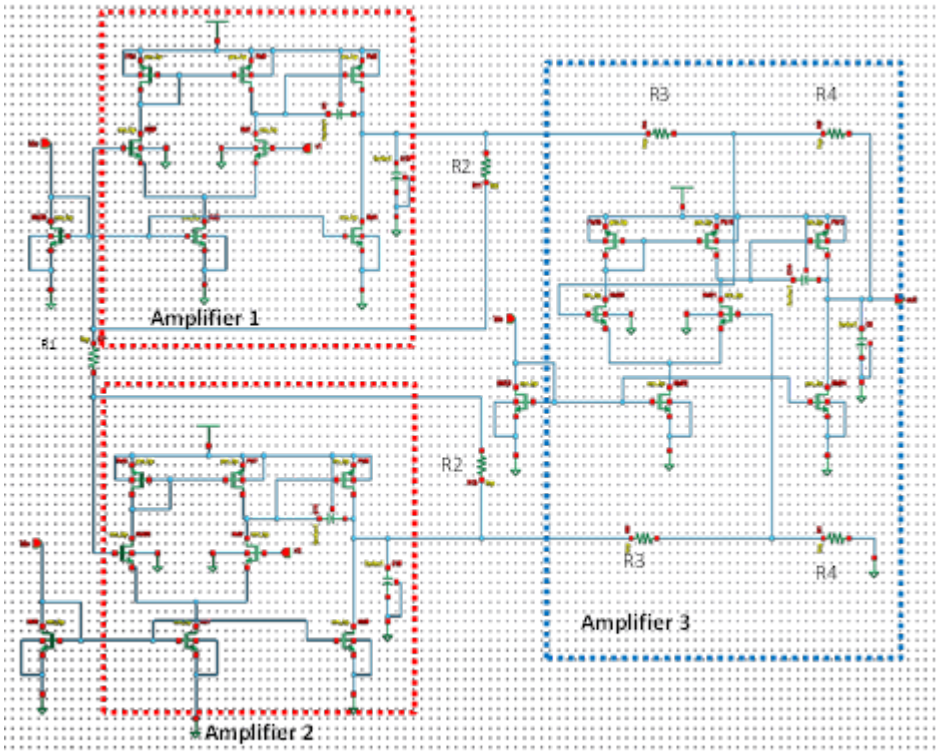


Fig. 4. Schematic diagram of proposed amplifier

The instrumentation amplifier is designed using the Miller-Compensation Technique. A capacitor is connected between the first stage and second stage of the circuit. The compensation capacitor is used to improve the frequency response as well as to decrease the slew rate. of the amplifier. The compensation technique can help to reduce the power consumption of the whole circuit as well as to suppress unwanted noise. To prevent the amplifier become unstable and the occurrence of under-

damped oscillatory time response, a two-stage op-amp is used and designed with a frequency compensation technique [2]. The most important characteristic of using this technique is to ensure the circuit remains stable [6,7].

B_{eff} is defined as the current in over current out of the transistors in DC. To obtain parameters of $\mu_n C_{ox}$ and $\mu_p C_{ox}$, B_{eff} is obtained through the simulation. B_{eff} for NMOS is 4.34 x10^{-3} which is approximately 4.50 x10^{-3} and B_{eff} for PMOS is 1.20 x10^{-3} which approximately 1.50 x10^{-3} is obtained through the simulation. From Eq. (1), the $\mu_n C_{ox}$ obtained is 450 μA/V^2, where the (W/L) of transistor is 10 and B_{eff} is 4.50 x10^{-3}. From Eq. (2), the $\mu_p C_{ox}$ obtained is 150 μA/V^2, where (W/L) is 10 and B_{eff} is 1.50 x10^{-3}. B_{eff} represents the beta effective, μ_n and μ_p are the mobility of electron and proton respectively, C_{ox} is the capacitance oxide while (W/L) is the ratio of width to length of transistors.

$$\mu_n C_{ox} \left(\frac{W}{L}\right) = B_{eff} \tag{1}$$

$$\mu_p C_{ox} \left(\frac{W}{L}\right) = B_{eff} \tag{2}$$

Some specifications are fixed for calculation and simulation processes that aim to get the width of the transistors as shown in Table 1. The threshold voltage of PMOS and NMOS is obtained through the simulation process to obtain the width and length of the transistors as shown in Table 2.

Table 1
Specifications for calculation purposes

Parameter	Value
Gain bandwidth, GBW	30 MHz
Slew rate, SR	20 V/μsec
Input common-mode range (max), $ICMR_{max}$	1.0 V
Input common-mode range (min), $ICMR_{min}$	0.5 V
Load capacitor, C_L	2 pF
Voltage supply, V_{dd}	1.2 V

Table 2
Threshold voltage for PMOS and NMOS

Threshold voltage	ICMR (max) = 1 V	ICMR (min) = 0.5 V
PMOS, V_{tp} (mV)	-319.0	-319.0
NMOS, V_{tn} (mV)	364.7	279.6

The capacitance of the compensation capacitor, C_L is obtained by using Eq. (3) and the compensation capacitor's capacitance obtained is 800 fF. C_L represents the load capacitor which is fixed to 2 pF as in Table 1. Next, current flow through the transistor M5 is obtained by using Eq. (4). From Eq. (4), the current flow through transistor M5, I_5 is $16\ \mu A$ which approximated to $20\ \mu A$ where slew rate, SR is $20\ V/\mu sec$.

$$Compensation\ capacitor, C_C = 0.22C_L \tag{3}$$

$$Slew\ rate, SR, = \frac{I5}{C_C} \tag{4}$$

Before obtaining the ratio of width to length of M1 and M2, the transconductance of M1 is obtained by using Eq. (5) with the value of 160 μS. GBW represents the gain bandwidth fixed in Table 1 and C_c represents the capacitance of the compensation capacitor. After the transconductance of

M1 is obtained, the ratio of width over the length of M1 and M2 is obtained through Eq. (6) with a value of 2.84 which is approximately 3. The current flow through M1, I_{d1} is 10 µA.

$$M1, g_{m1} = GBW\ x\ Cc\ x\ 2\pi \tag{5}$$

$$\left(\frac{W}{L}\right)_{1,2} = \frac{(g_{m1})^2}{(\mu_n C_{ox})(2I_{d1})} \tag{6}$$

From Eq. (7), the ratio of width to length of M3 and M4 obtained is 5.21 (approximated to 6). V_{dd} represents the voltage supplied to the amplifier, ICMR $_{(max)}$ represents the maximum input common-mode range which is fixed in Table 1, I_{d3} is the current flow through M3. $V_{t3(max)}$ and $V_{t1(min)}$ stand for the maximum and minimum threshold voltage for M3 and M1.

$$\left(\frac{W}{L}\right)_{3,4} = \frac{2I_{d3}}{(\mu_P C_{OX})(V_{dd} - ICMR_{max} - V_{t3(max)} + V_{t1(min)})^2} \tag{7}$$

The saturation voltage of transistor M5 is computed from Eq. (8) with the value of 0.018 V. However, if saturation voltage was below 100 mA, the transistor will operate at the triode region. Adjustment of the ratio of width to the length of transistors M1 and M2 is made. The ratio is changed to 28 and the saturation voltage obtained is 0.1002 V. ICMR $_{(min)}$ represents the minimum input common-mode range. After the important parameters are obtained, the ratio of width to length of transistor M5 and transistor M6 is computed from Eq. (9) which is 8.85 and approximated to 9.

$$V_{DSAT} = ICMR(min) - \sqrt{\frac{2I_{d1}}{\mu_n C_{ox}(W/L)_{1,2}}} - V_{t1max} \tag{8}$$

$$\left(\frac{W}{L}\right)_{5,6} = \frac{2I_{d5}}{(\mu_n C_{ox})(V_{DSAT})^2} \tag{9}$$

Before obtaining the ratio of width to length of transistors M7, the transconductance of transistors M4 and M7 is obtained by using Eq. (10) and Eq. (11) respectively with the value of 134 µS and 1600 µS. From Eq. (12), the ratio of width over the length of transistors M7 is approximately 72.

$$g_{m4} = \sqrt{(\mu_p C_{ox})\ x\ (\frac{W}{L})_{3,4}\ x\ 2I_{d4}} \tag{10}$$

$$g_{m7} = 10 g_{m1} \tag{11}$$

$$(\frac{W}{L})_7 = \frac{g_{m7}}{g_{m4}} x (\frac{W}{L})_4 \tag{12}$$

The current flow through the transistor M7 is computed from Eq. (13) which is 120 µA. Based on Eq. (14), the transistor's width to length ratio is computed with (W/L) of 54.

$$I_7 = \frac{(\frac{W}{L})_7}{(\frac{W}{L})_4} x\ I_4 \tag{13}$$

$$\left(\frac{W}{L}\right)_8 = \frac{I_7}{I_5} x \left(\frac{W}{L}\right)_5 \quad (14)$$

Table 3 shows the width and length of the transistors for the designed amplifier, the length of all the transistors fixed at 500 nm. The ratio of width to length of transistor M1 and M2 is 28, M3 and M4 are 6, M5 and M6 is 9 M7 and M8 is 72 and 54 respectively. Table 4 lists the resistance for each of the resistors used for the designed amplifier to meet the requirement as predetermined.

Table 3
Width and length of the transistor

Transistor	Width and length
M1, M2	L=500 nm W=14 µm
M3, M4	L=500 nm W=3 µm
M5, M6	L=500 nm W=4.5 µm
M7	L=500 nm W=36 µm
M8	L=500 nm W=27 µm

Table 4
Proposed resistor value

Resistor	Resistance (kΩ)
R1	3
R2	100
R3	3
R4	100

3. Result

The differential gain of the proposed instrumentation amplifier during pre-layout simulation is shown in Figure 5. The theoretical gain obtained is 67.07 dB. After the pre-layout simulation is carried out, the differential gain of the proposed instrumentation amplifier is 64.15 dB. The cut off frequency of the designed amplifier is 75.9 kHz.

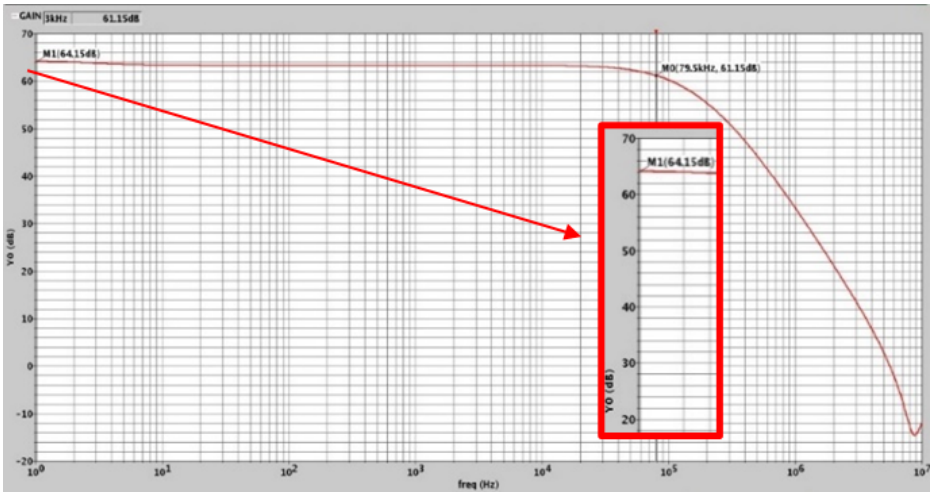


Fig. 5. Differential gain of the proposed instrumentation amplifier (pre-layout)

Total power dissipation comprises static power dissipation as well as dynamic power dissipation. Static power dissipation will occur because of the leakage of current while the occurrence of dynamic power dissipation is due to the charging and discharging of the transistor dissipation. When the static power dissipation and the dynamic power dissipation of transistors are decreased, the total power dissipation for the whole circuit will also be reduced. This can be done by lowering the power supply for the whole circuit. It is because static power dissipation is directly proportional to the power supply. The power dissipation of the proposed instrumentation amplifier measured is 115.6 µW as shown in Figure 6.

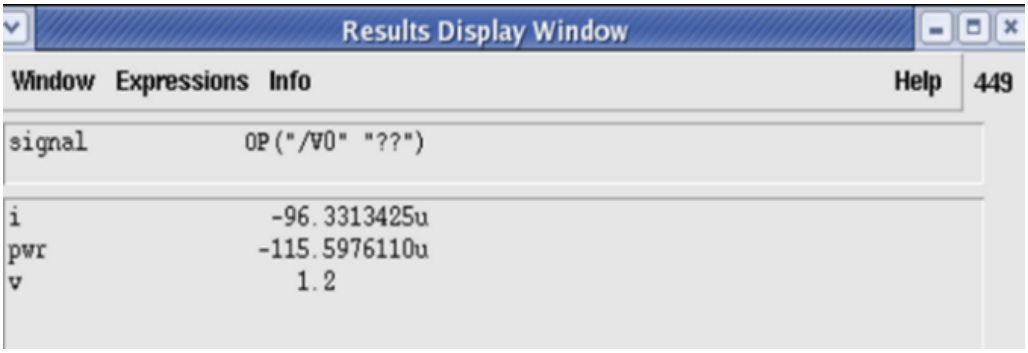


Fig. 6. Power dissipation of instrumentation amplifier (pre-layout)

Input referred noise is the combination of flicker noise as well as thermal noise. But will concentrate more on the flicker noise since noise in the surrounding will affect the biomedical signal because the signal is very low frequency and low amplitude. Flicker noise varies accordingly by the changes of width and length of the transistor [7]. From the simulation result, the input-referred noise of the instrumentation amplifier measured is 10.41 µ(V/√Hz) as shown in Figure 7. K is the transistor flicker noise factor, *f* stands for the frequency of the signal, (W/L) represents the ratio of width to length of the transistors and C_{ox} stands for the gate capacitance per unit area.

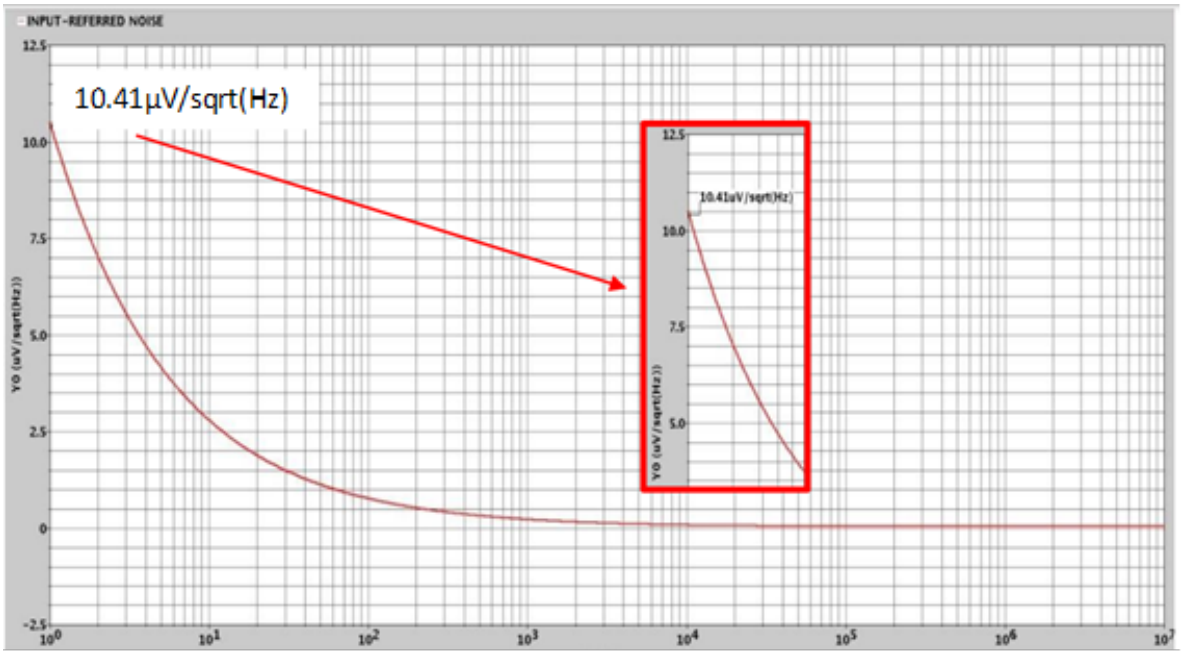


Fig. 7. Input referred noise of instrumentation amplifier (pre-layout)

The common-mode gain measured is -43.1 dB as shown in Figure 8. There is a "bum" shape occurred at around frequency of 10^5 Hz due to the occurrence of fluctuation. The differential gain measured is 64.15 dB as shown in Figure 5. Therefore, the CMRR of the proposed instrumentation amplifier measured is 107.25 dB by calculating using Eq. (15). A_D represents the differential gain of the amplifier while A_C represents the common-mode gain of the amplifier.

$$CMRR = 20log(\frac{A_D}{A_C}) \quad (15)$$

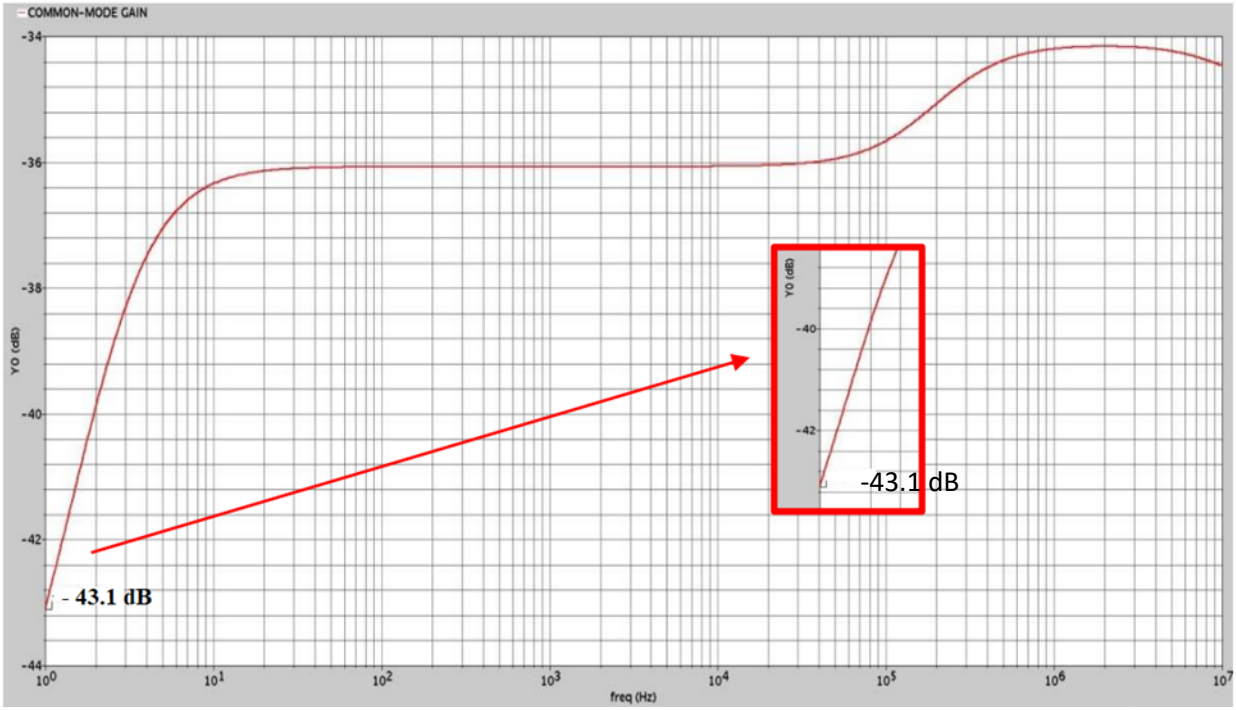


Fig. 8. Common mode gain of the instrumentation amplifier (pre-layout)

Figure 9 shows the layout of the proposed instrumentation amplifier for biomedical applications. Post-layout simulation is carried out right after the *Calibre* of design rule check (DRC), layout versus schematic (LVS), and parasitic extraction (PEX) with no occurrence of any errors. Through the post-layout simulation, all the design constraints will be verified. Post-layout simulation is considered an important step before it prepares for the fabrication process.

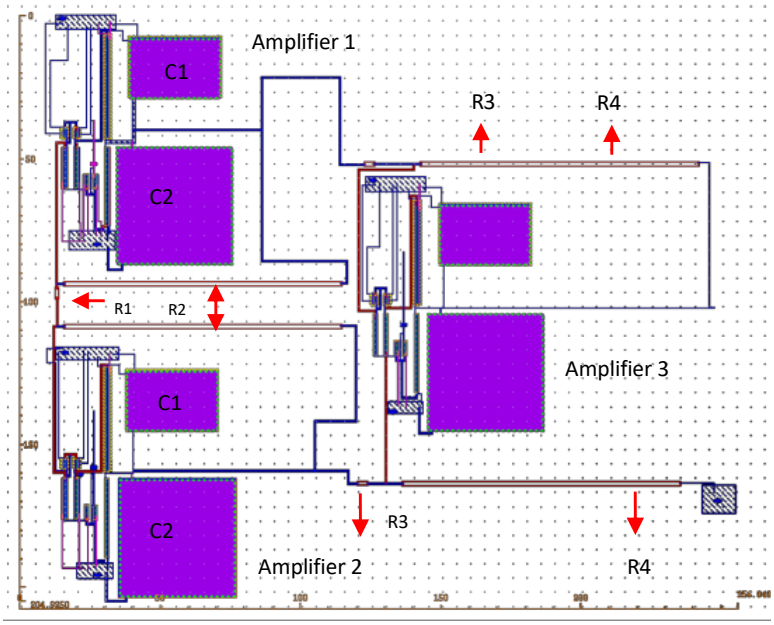


Fig. 9. Layout of proposed instrumentation amplifier

During post-layout simulation, a more precise analog model design can be created with the extracted parasitic capacitance and resistance. Method of design the layout such as width or length of the transistors, finger of transistors, etc will affect the performance of the designed circuit. The width and length of the transistor will affect the current flow. Once the current flow is low, the performance of the circuit will degrade. Thus, there will occur a slight difference between the pre-layout simulation and the post-layout simulation results. The differential gain of the proposed instrumentation amplifier obtained in post-layout simulation is 63.69 dB as shown in Figure 10.

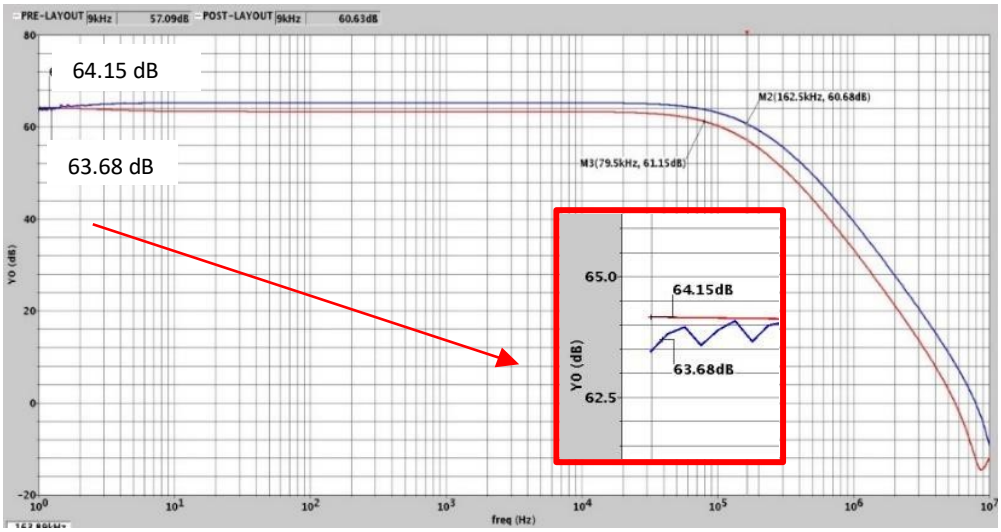


Fig. 10. Differential gain of the instrumentation amplifier (pre-layout & post-layout)

The cutoff frequency obtained in pre-layout simulation is 79.5 kHz and 162.5 kHz in post-layout simulation. The input-referred noise of the designed instrumentation amplifier acquired from the post-layout simulation is 10.52 µ(V/$\sqrt{}$ Hz) as shown in Figure 11. Input referred noise of the proposed instrumentation amplifier which was acquired from the pre-layout simulation is 10.41 µ(V/√Hz) and 10.52 µ(V/√Hz) from the post-layout simulation result. The difference between pre-layout simulation and post-layout results is 0.11 µ(V/√Hz) which is equivalent to 1%. Thus, the input-referred noise of

the proposed amplifier in pre-layout and post-layout simulation is almost identical. Both outcomes of the pre-layout and post-layout simulation meet the requirement of the design specification. The difference between pre-layout and post-layout simulation is due to the parasitic effect. The parasitic effect is varied based on the technique of the layout design. Thus, the difference between pre-layout and post-layout simulation results can be debugged by making changes to the technique of creating the layout.

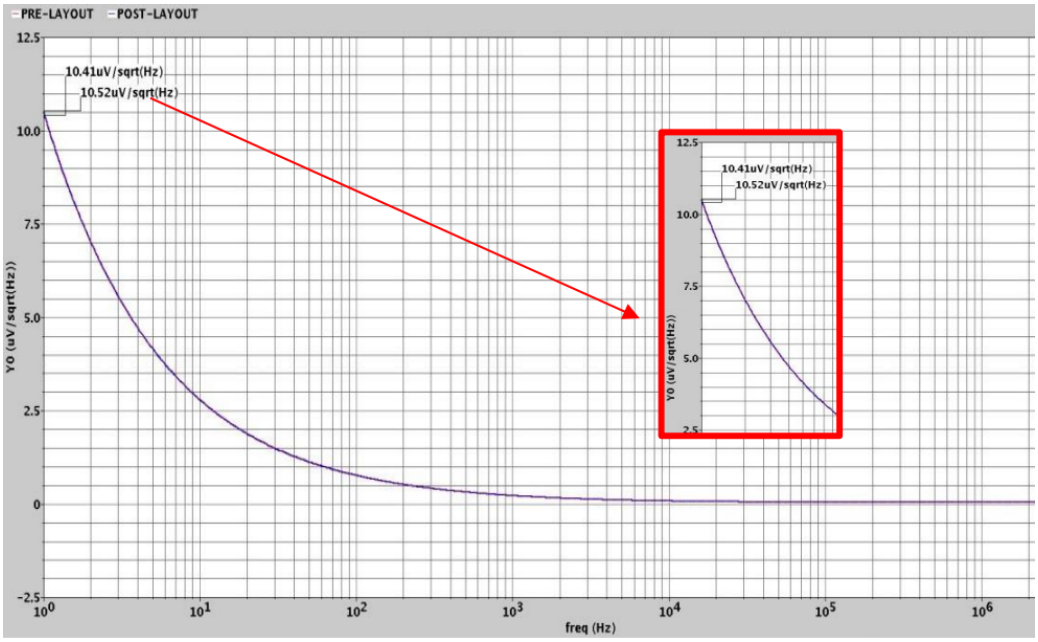


Fig. 11. Input referred to noise of instrumentation amplifier (pre-layout & post-layout)

The measured differential gain in pre-layout and post-layout simulation is 64.15 dB and 63.69 dB respectively. According to Figure 12, the common-mode gain of the instrumentation amplifier design obtained from the pre-layout simulation is -43.1 dB while the common-mode gain of the post-layout simulation is -36.7 dB. Thus, the CMRR of the proposed design was obtained from pre-layout simulation resulting in 107.25 dB and 100.39 dB from post-layout simulation.

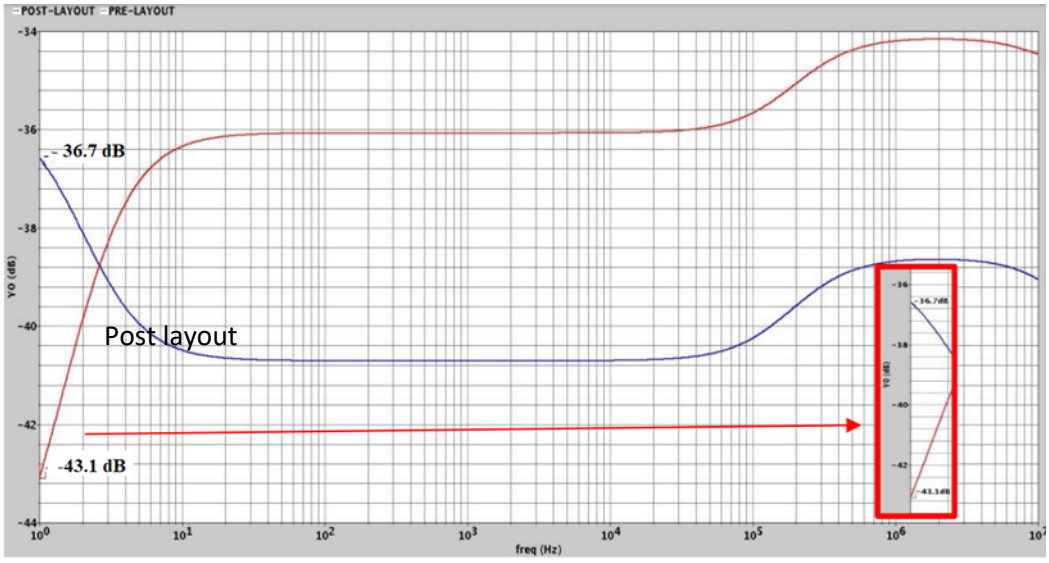


Fig. 12. Common mode gain of the instrumentation amplifier (pre-layout & post-layout)

Figure 13 displays the power dissipation of the proposed instrumentation amplifier obtained from post-layout simulation which is 115.57 µW. The parasitic netlist for resistors and capacitors in the instrumentation amplifier layout was obtained as illustrated in Figure 14.

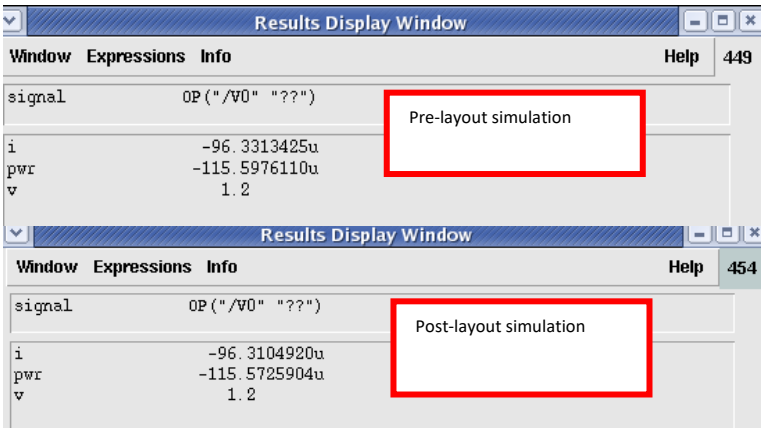
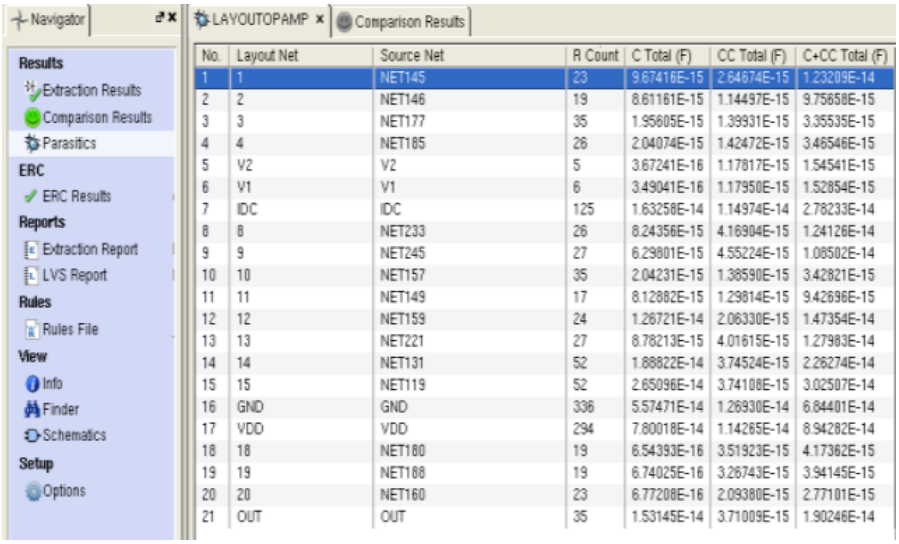


Fig. 13. Power dissipation of instrumentation amplifier (pre-layout & post-layout)



No.	Layout Net	Source Net	R Count	C Total (F)	CC Total (F)	C+CC Total (F)
1	1	NET145	23	9.67416E-15	2.64874E-15	1.23209E-14
2	2	NET146	19	8.61161E-15	1.14497E-15	9.75658E-15
3	3	NET177	35	1.95605E-15	1.39931E-15	3.35535E-15
4	4	NET185	26	2.04074E-15	1.42472E-15	3.46546E-15
5	V2	V2	5	3.67241E-16	1.17817E-15	1.54541E-15
6	V1	V1	6	3.49041E-16	1.17950E-15	1.52854E-15
7	IDC	IDC	125	1.63258E-14	1.14974E-14	2.78233E-14
8	8	NET233	26	8.24356E-15	4.16904E-15	1.24126E-14
9	9	NET245	27	6.29801E-15	4.55224E-15	1.08502E-14
10	10	NET157	35	2.04231E-15	1.38590E-15	3.42821E-15
11	11	NET149	17	8.12882E-15	1.29814E-15	9.42696E-15
12	12	NET159	24	1.26721E-14	2.06330E-15	1.47354E-14
13	13	NET221	27	8.78213E-15	4.01615E-15	1.27983E-14
14	14	NET131	52	1.88822E-14	3.74524E-15	2.26274E-14
15	15	NET119	52	2.65096E-14	3.74108E-15	3.02507E-14
16	GND	GND	336	5.57471E-14	1.26930E-14	6.84401E-14
17	VDD	VDD	294	7.80018E-14	1.14265E-14	8.94282E-14
18	18	NET180	19	6.54393E-16	3.51923E-15	4.17362E-15
19	19	NET188	19	6.74025E-16	3.26743E-15	3.94145E-15
20	20	NET160	23	6.77208E-16	2.09380E-15	2.77101E-15
21	OUT	OUT	35	1.53145E-14	3.71009E-15	1.90246E-14

Fig. 14. Parasitic of the layout of instrumentation amplifier circuit

Table 5 shows a comparison between the proposed value, pre-layout as well as post-layout simulation value. The value of pre-layout simulation and post-layout simulation has a small difference, but it is still acceptable. The small difference is due to the technique used to create the layout by varying the number of fingers of the components which can affect the performance of the whole circuit, and the width or length of the transistor also may affect the result.

Table 5
Comparison between proposed value, pre-layout and post-layout simulation value

	Proposed value	**Pre-layout simulation**	**Post-layout simulation**
Technology used (nm)	130		
Voltage supply (V)	1.2		
Gain (dB)	Above 60	64.15	63.69
Power dissipation (W)	Below 388µ	115.6µ	115.6µ
Input referred noise (V/$\sqrt{}$Hz)	Below 22.8m	10.41µ	10.52µ
CMRR (dB)	Above 100	107.25	100.39

The width and length of the transistor will affect the current flow. Once the current flow is low, the performance of the circuit will degrade. Apart from that, post-layout simulation has included parasitic capacitances which can provide a more precise analog model. However, parasitic capacitances affect the performance of the proposed instrumentation amplifier.

4. Conclusion

The proposed 130nm CMOS-based instrumentation amplifier is constructed successfully using Cadence Software and the simulation results also achieved the desired value. The circuit was designed to fit in the energy harvesting application in biomedical devices. The gain of the designed amplifier for pre-layout simulation achieved is 64.15 dB with input-referred noise of 10.41 μ(V/$\sqrt{}$Hz) and power dissipation of 115.6 μW as well as the CMRR of the amplifier designed is 107.25 dB. Additionally, the gain of the amplifier for post-layout simulation achieved approximately 64 dB with input-referred noise of 10.52 μ(V/$\sqrt{}$Hz), the power dissipation of 115.6 μW, and CMRR of 100.39 dB. Apart from that, the amplifier is designed with overall layout size of 5.25x104 μm^2.

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